PROFIBUS RS-485 TRANSCEIVERS

FEATURES

- **Optimized for PROFIBUS Networks**
  - **Signaling Rates Up to 40 Mbps**
  - **Differential Output Exceeds 2.1 V (54 Ω Load)**
  - **Low Bus Capacitance of 10 pF (Max)**
- **Meets the Requirements of TIA/EIA-485-A**
- **ESD Protection Exceeds ±10 kV HBM**
- **Failsafe Receiver for Bus Open, Short, Idle**
- **Up to 160 Transceivers on a Bus**
- **Low Skew During Output Transitions and Driver Enabling / Disabling**
- **Common-Mode Rejection Up to 50 MHz**
- **Short-Circuit Current Limit**
- **Hot Swap Capable**
- **Thermal Shutdown Protection**

APPLICATIONS

- **Process Automation**
  - **Chemical Production**
  - **Brewing and Distillation**
  - **Paper Mills**
- **Factory Automation**
  - **Automobile Production**
  - **Rolling, Pressing, Stamping Machines**
  - **Networked Sensors**
- **General RS-485 Networks**
  - **Motor/Motion Control**
  - **HVAC and Building Automation Networks**
  - **Networked Security Stations**

DESCRIPTION

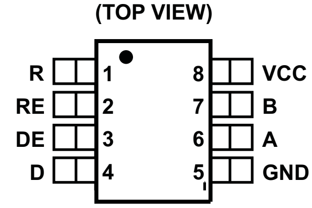
These devices are half-duplex differential transceivers, with characteristics optimized for use in PROFIBUS (EN 50170) applications. The driver output differential voltage exceeds the Profibus requirements of 2.1 V with a 54 Ω load. A signaling rate of up to 40 Mbps allows technology growth to high data transfer speeds. The low bus capacitance provides low signal distortion.

The SN65HVD1176 and SN75HVD1176 meet or exceed the requirements of ANSI standard TIA/EIA-485-A (RS-485) for differential data transmission across twisted-pair networks. The driver outputs and receiver inputs are tied together to form a half-duplex bus port, with one-fifth unit load, allowing up to 160 nodes on a single bus. The receiver output stays at logic high when the bus lines are shorted, left open, or when no driver is active. The driver outputs are in high impedance when the supply voltage is below 2.5 V to prevent bus disturbance during power cycling or during live insertion to the bus. An internal current limit protects the transceiver bus pins in short-circuit fault conditions by limiting the output current to a constant value. Thermal shutdown circuitry protects the device against damage due to excessive power dissipation caused by faulty loading and drive conditions.

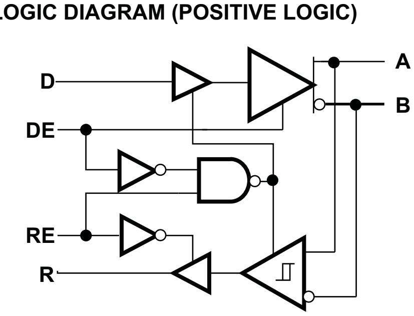
The SN75HVD1176 is characterized for operation at temperatures from 0°C to 70°C. The SN65HVD1176 is characterized for operation at temperatures from -40°C to 85°C.

For an isolated version of this device, see the ISO1176 (SLLS897) with integrated digital isolators.

D PACKAGE (TOP VIEW)



LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES(1)	PACKAGE MARKING(2)
0C to 70C	SN75HVD1176D	VN1176
-40°C to 85°C	SN65HVD1176D	VP1176

(1) The D package is available taped and reeled. Add an R suffix to the device type (for example, SN65HVD1176DR).
(2) For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted(1)

				SN65HVD1176 SN75HVD1176	UNIT
V_{CC}	Supply voltage(2)			–0.5 to 7	V
	Voltage at any bus I/O terminal			–9 to 14	V
	Voltage input, transient pulse, A and B, (through 100 Ω, see Figure 15)			–40 to 40	V
	Voltage input at any D, DE or $\overline{RE}$ terminal			–0.5 to 7	V
I_O	Receiver output current			–10 to 10	mA
	Electrostatic discharge	Human Body Model, (HBM)(3)	All pins	4	kV
			Bus terminals and GND	10	kV
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal..
(3) Tested in accordance with JEDEC standard 22. test method A114-A..

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	V
V_{IL}	Differential input voltage	A with respect to B	-12		12	V
I_O	Output current	Driver	-70		70	mA
		Receiver	-8		8	mA
T_J	Junction temperature (1)	SN65HVD1176	-40		130	°C
		SN75HVD1176	0		130	°C
R_L	Differential load resistance		54			Ω
$1/t_{U1}$	Signaling rate				40	Mbps

(1) See the Thermal Characteristics table for more information on maintenance of this requirement.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER							
V_O	Open-circuit output voltage	A or B,	No load	0		V_{CC}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude	RL = 54 Ω	See Figure 1	2.1	2.9		V
		With common-mode loading, (V_{TEST} from -7 V to 12 V) See Figure 2		2.1	2.7		V
$\Delta\|V_{OD(SS)}\|$	Change in steady-state differential output voltage between logic states	See Figure 1 and Figure 6		–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 5		2	2.5	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			–0.2	0	0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				0.5		V
$V_{OD(RING)}$	Differential output voltage over and under shoot	R_L = 54 Ω, C_L = 50 pF, See Figure 6				10%	$V_{OD(PP)}$
I_I	Input current	D, DE		-50		50	µA
$I_{O(OFF)}$	Output current with power off	V_{CC} ≤ 2.5 V		See receiver line input			
I_{OZ}	High impedance state output current	DE at 0 V					
$I_{OS(P)}$	Peak short-circuit output current	DE at V_{CC}, See Figure 8	V_{OS} = –7 V to 12 V	-250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current		V_{OS} > 4 V, Output driving low	60	90	135	mA
			VOS < 1 V, Output driving high	-135	-90	-60	mA
C_{OD}	Differential output capacitance			See receiver C_{ID}			pF
RECEIVER							
$V_{IT(+)}$	Positive-going differential input voltage threshold	SeeFigure 9	V_O = 2.4 V, I_O = –8 mA		–80	–20	mV
$V_{IT(–)}$	Negative-going differential input voltage threshold		V_O = 0.4 V, I_O = 8 mA	-200	-120		mV
V_{HYS}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)				40		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See Figure 9		4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, See Figure 9			0.2	0.4	V
I_A, I_B	Bus pin input current	V_I = - 7 V to 12 V, Other input = 0 V	V_{CC} = 4.75 V to 5.25 V	–160		200	µA
$I_{A(OFF)}$ $I_{B(OFF)}$			V_{CC} = 0 V				
I_I	Receiver enable input current	$\overline{RE}$		–50		50	µA
I_{OZ}	High-impedance - state output current	$\overline{RE}$ = V_{CC}		–1		1	µA
R_I	Input resistance			60			kΩ
C_{ID}	Differential input capacitance	Test input signal is a 1.5 MHz sine wave with amplitude 1 V_{PP}, capacitance measured across A and B			7	10	pF
C_{MR}	Common mode rejection	See Figure 11			4		V

(1) All typical values are at V_{CC} = 5 V and 25°C.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
DRIVER							
t_{PLH}	Propagation delay time low-level-to-high-level output	RL = 54 Ω, C_L = 50 pF, See Figure 3		4	7	10	ns
t_{PHL}	Propagation delay time high-level-to-low-level output			4	7	10	ns
$t_{sk(p)}$	Pulse skew | t_{PLH} – t_{PHL} |				0	2	ns
t_r	Differential output rise time			2	3	7.5	ns
t_f	Differential output fall time			2	3	7.5	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew	See Figure 4			0.2	1	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output	R_L = 110 Ω, C_L = 50 pF See Figure 7	$\overline{RE}$ at 0 V		10	20	ns
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-to- high-impedance output				10	20	ns
$\|t_{p(AZL)} - t_{p(BZH)}\|$ $\|t_{p(AZH)} - t_{p(BZL)}\|$	Enable skew time				0.55	1.5	ns
$\|t_{p(ALZ)} - t_{p(BHZ)}\|$ $\|t_{p(AHZ)} - t_{p(BLZ)}\|$	Disable skew time					2.5	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output (from sleep mode)		$\overline{RE}$ at 5 V		1	4	µs
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-output-to high-impedance (to sleep mode)				30	50	ns
$t_{(CFB)}$	Time from application of short-circuit to current foldback	See Figure 8			0.5		µs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown	T_A = 25°C, See Figure 8		100			µs
RECEIVER							
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 10			20	25	ns
t_{PHL}	Propagation delay time, high-to-low level output				20	25	ns
$t_{sk(p)}$	Pulse skew | t_{PLH} – t_{PHL} |				1	2	ns
t_r	Receiver output voltage rise time				2	4	ns
t_f	Receiver output voltage fall time				2	4	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	DE at V_{CC}, See Figure 13				20	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output					20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	DE at V_{CC}, See Figure 14				20	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output					20	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output (standby to active)	DE at 0 V, See Figure 12			1	4	µs
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output (active to standby)				13	20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output (standby to active)	DE at 0 V, See Figure 12			2	4	µs
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output (active to standby)				13	20	ns

(1) All typical values are at V_{CC} = 5 V and 25°C.

Table 1. SUPPLY CURRENT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply Current[(1)]	Driver and receiver, $\overline{RE}$ at 0 V, DE at V_{CC}, All other inputs open, no load		4	6	mA
		Driver only, $\overline{RE}$ at V_{CC}, DE at V_{CC}, All other inputs open, no load		3.8	6	mA
		Receiver only, $\overline{RE}$ at 0 V, DE at 0 V, All other inputs open, no load		3.6	6	mA
		Standby only, $\overline{RE}$ at V_{CC}, DE at 0 V, All other inputs open		0.2	5	µA

(1) Over recommended operating conditions

THERMAL CHARACTERISTICS[(1)]

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[(2)]	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[(3)]		Low-K board[(4)], no air flow		208.3		°C/W
			High-K board[(5)], no air flow		128.7		°C/W
θ_{JB}	Junction-to-board thermal resistance		High-K board		77.6		°C/W
θ_{JC}	Junction-to-case thermal resistance				43.9		°C/W
P_D	Device power dissipation		R_L = 54 Ω, C_L = 50 pF, 0 V to 3 V, 15 MHz, 50% duty cycle square wave input, driver and receiver enabled		277	318	mW
T_A	Ambient air temperature	SN65HVD1176	Low-K board, no air flow, P_D = 318 mW	–40		64	°C
		SN75HVD1176		0			°C
		SN65HVD1176	High-K board, no air flow, P_D = 318 mW	–40		89	°C
		SN75HVD1176		0			°C
T_{SD}	Thermal shut down junction temperature				150		°C

(1) See Application Information section for an explanation of these parameters.
(2) All typical values are with V_{CC} = 5 V and T_A = 25°C.
(3) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
(4) JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.
(5) JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

PARAMETER MEASUREMENT INFORMATION

NOTE:

Test load capacitance includes probe and jig capacitance (unless otherwise specified).

Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle, Z_o = 50 Ω (unless otherwise specified).

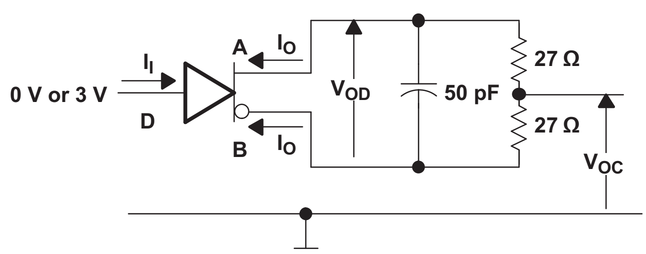


Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

PARAMETER MEASUREMENT INFORMATION (continued)

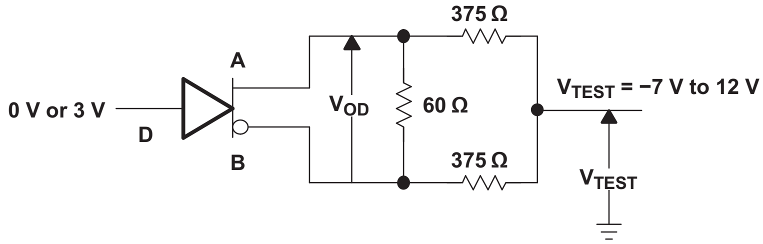


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

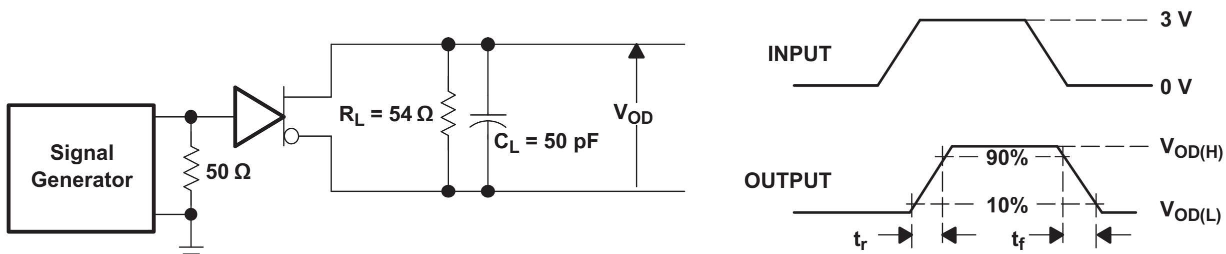


Figure 3. Driver Switching Test Circuit and Rise/Fall Time Measurement

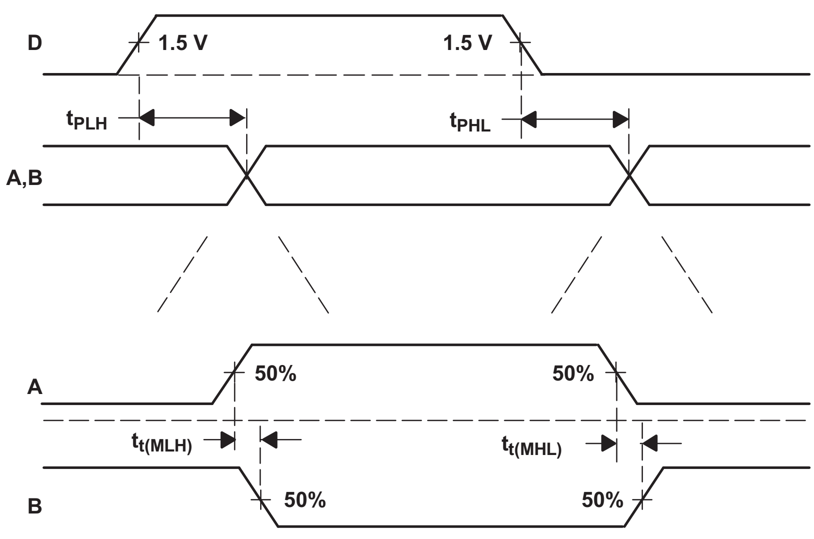


Figure 4. Driver Switching Waveforms for Propagation Delay and Output Midpoint Time Measurements

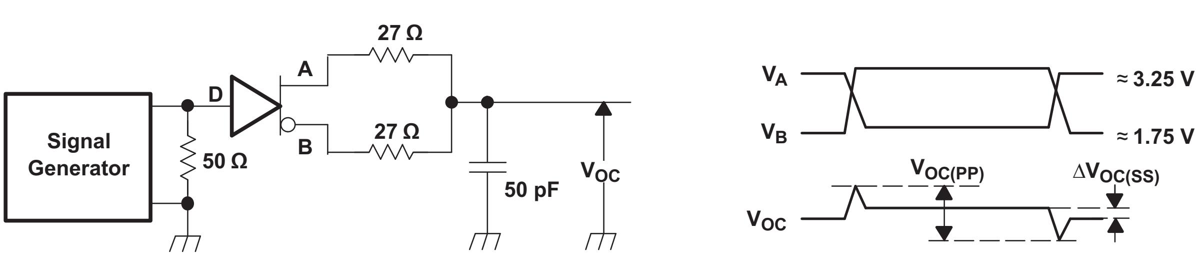
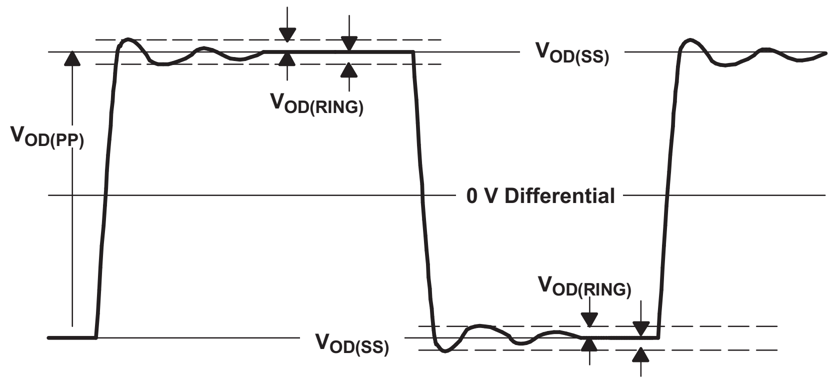


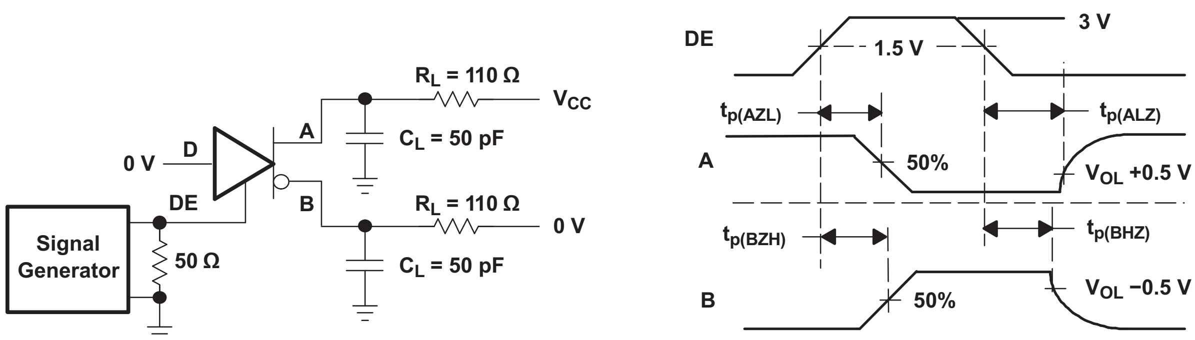
Figure 5. Driver V_{OC} Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

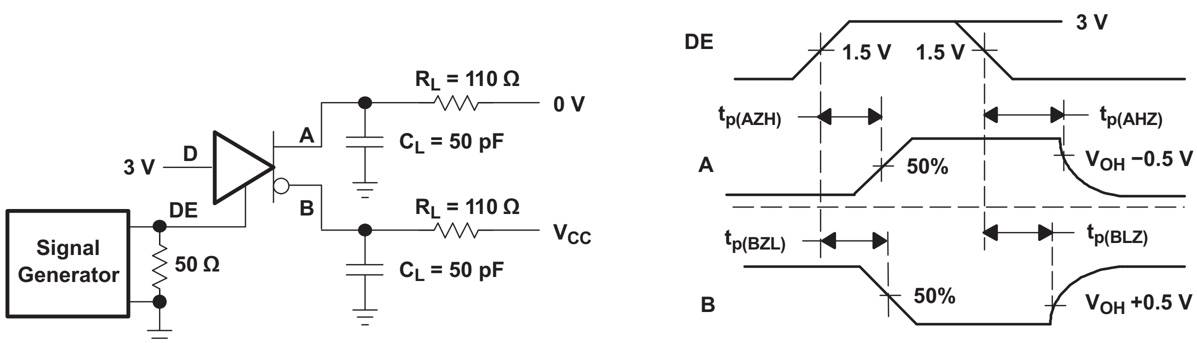


(1) $V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

Figure 6. $V_{OD(RING)}$ Waveform and Definitions



a) D at Logic Low



b) D at Logic High

Figure 7. Driver Enable/Disable Test

PARAMETER MEASUREMENT INFORMATION (continued)

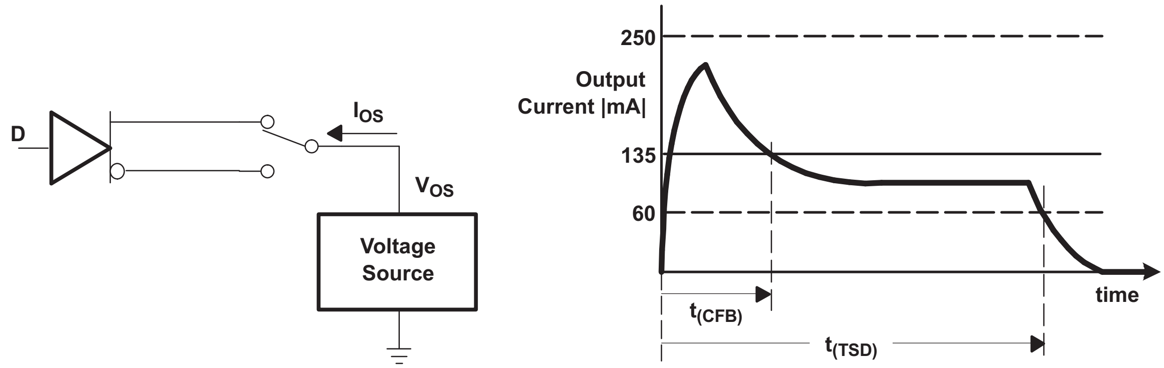


Figure 8. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t = 0)

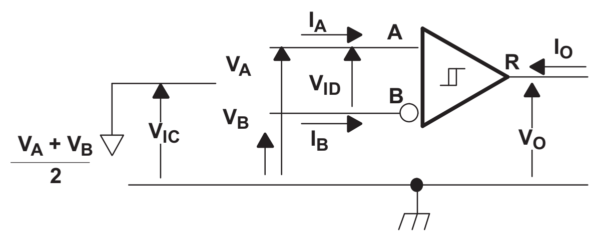


Figure 9. Receiver DC Parameter Definitions

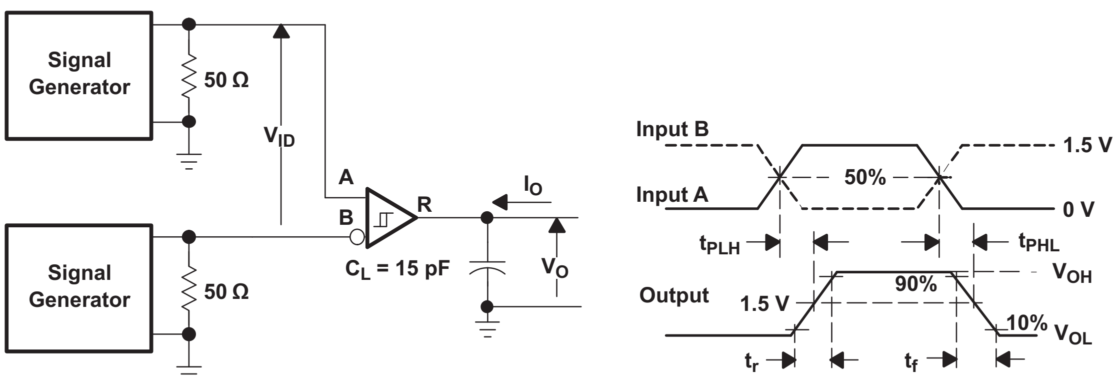


Figure 10. Receiver Switching Test Circuit and Waveforms

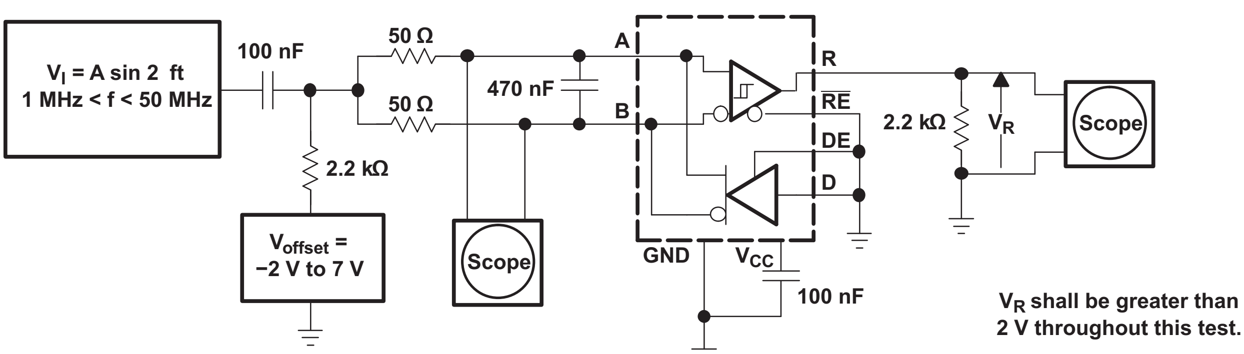


Figure 11. Receiver Common-Mode Rejection Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

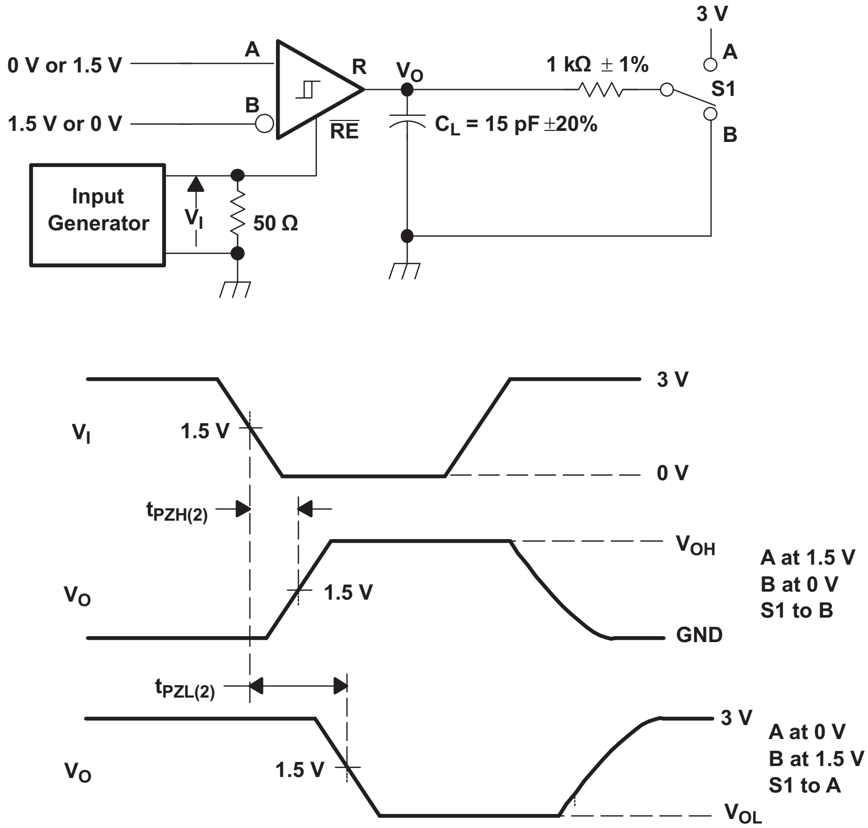


Figure 12. Receiver Enable Time From Standby (Driver Disabled)

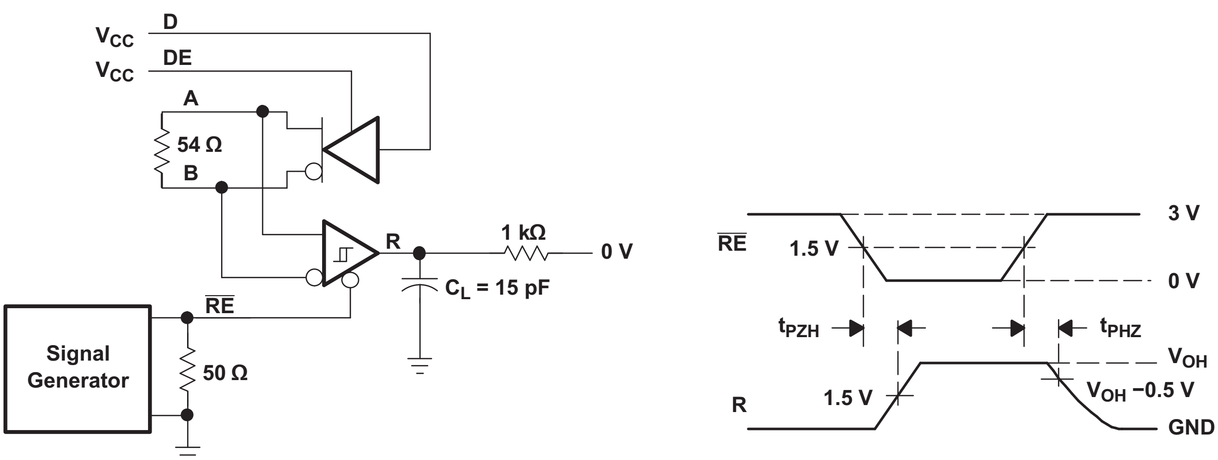


Figure 13. Receiver Enable Test Circuit and Waveforms, Data Output High (Driver Active)

PARAMETER MEASUREMENT INFORMATION (continued)

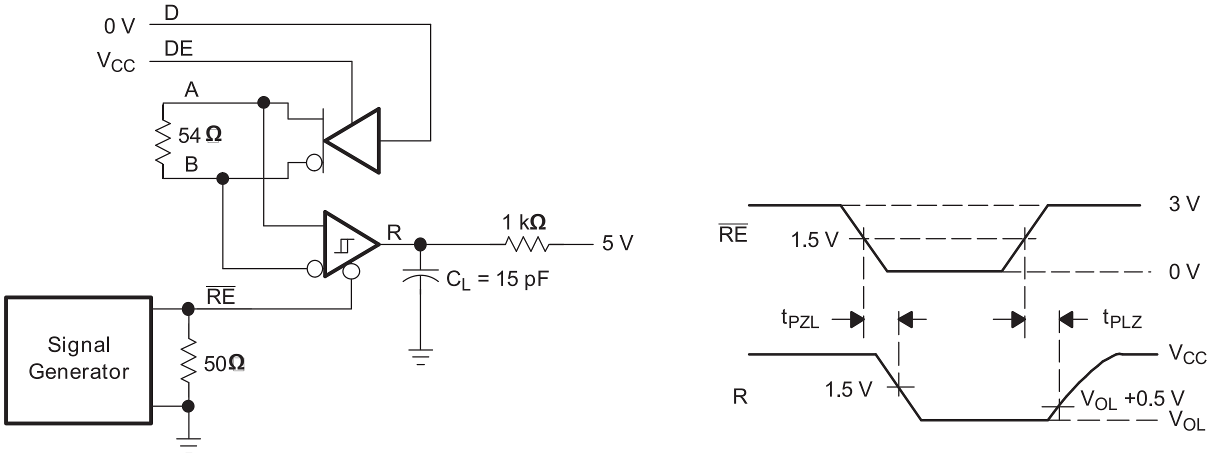


Figure 14. Receiver Enable Test Circuit and Waveforms, Data Output Low (Driver Active)

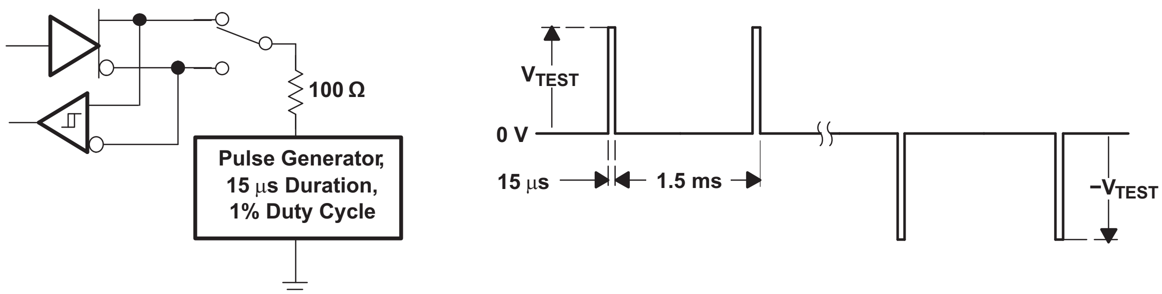


Figure 15. Test Circuit and Waveforms, Transient Overvoltage Test

DEVICE INFORMATION

Table 2. Driver Function Table(1)

INPUT	ENABLE	OUTPUTS	
D	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	H	L

(1) **H** = high level, **L** = low level, **X** = don't care, **Z** = high impedance (off)

Table 3. Receiver Function Table(1)

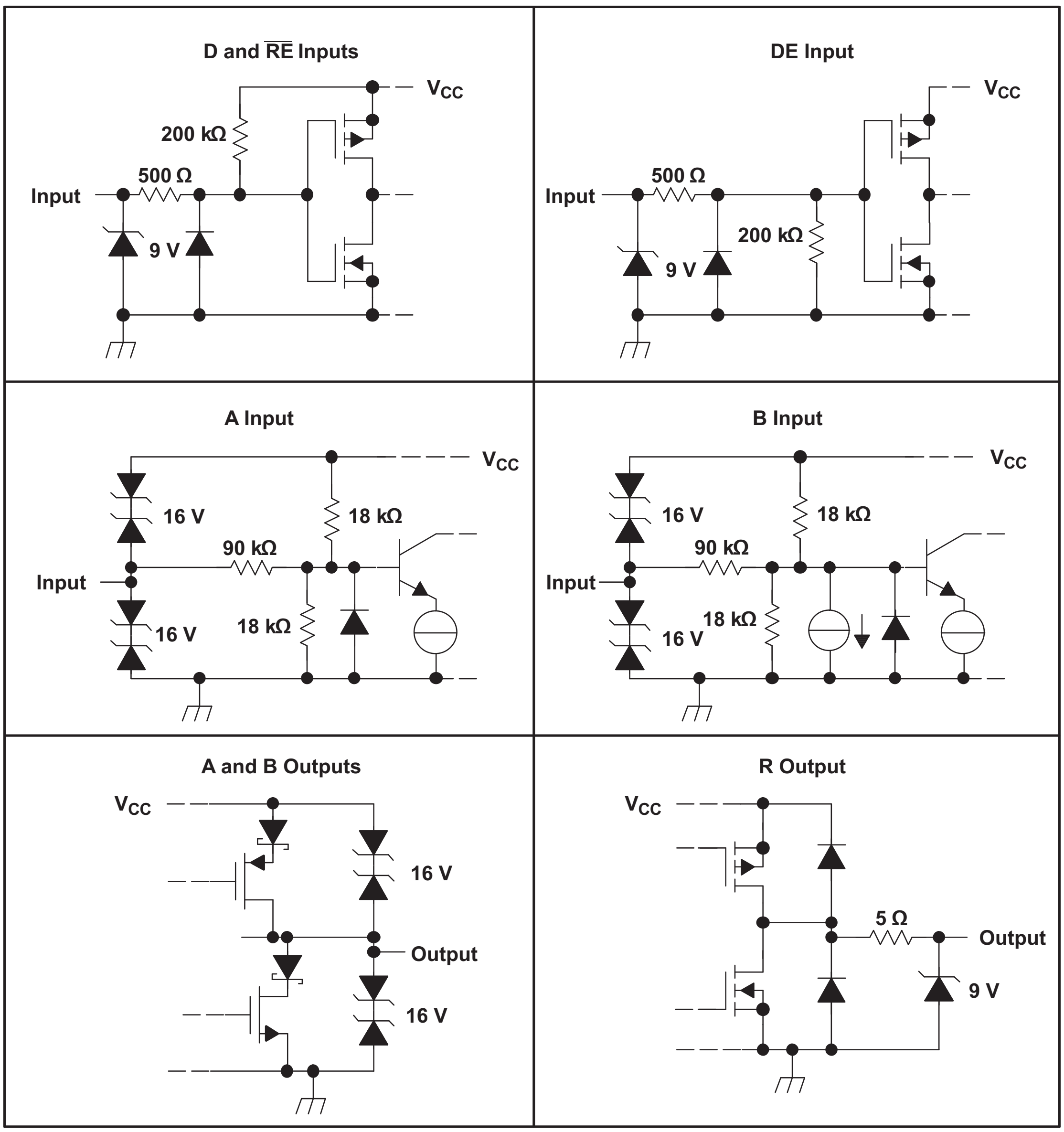
DIFFRENTIAL INPUT $V_{ID} = (V_A – V_B)$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.02$ V	L	H

(1) **H** = high level, **L** = low level, **X** = don't care, **Z** = high impedance (off), **?** = indeterminate

Table 3. Receiver Function Table (continued)

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
$-0.2\ V < V_{ID} < -0.02\ V$	L	?
$V_{ID} \le -0.2\ V$	L	L
X	H	Z
X	OPEN	Z
Open Circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE
vs
LOAD CURRENT

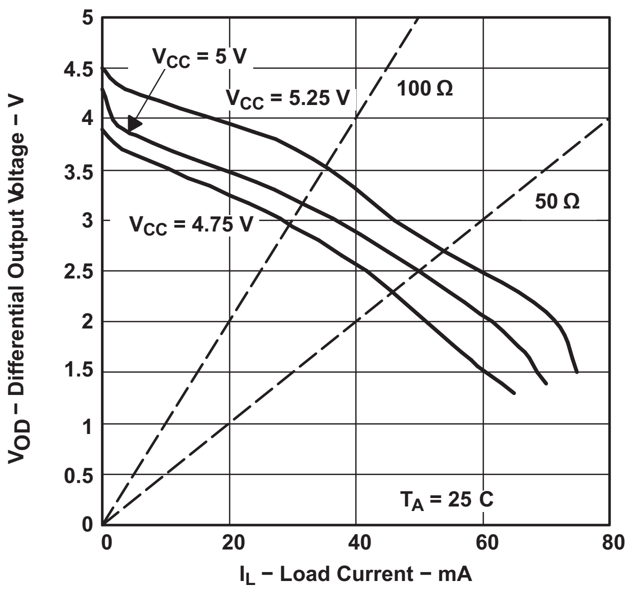


Figure 16.

DRIVER SUPPLY CURRENT
vs
SIGNALING RATE

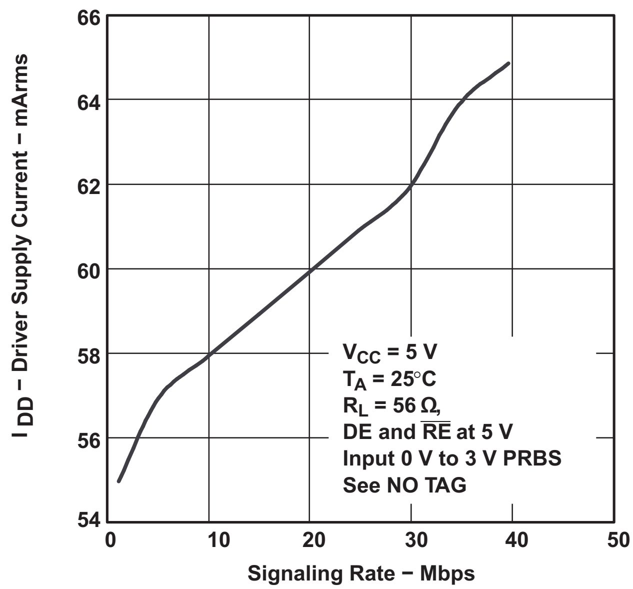


Figure 17.

DRIVER OUTPUT TRANSITION SKEW
vs
FREE-AIR TEMPERATURE

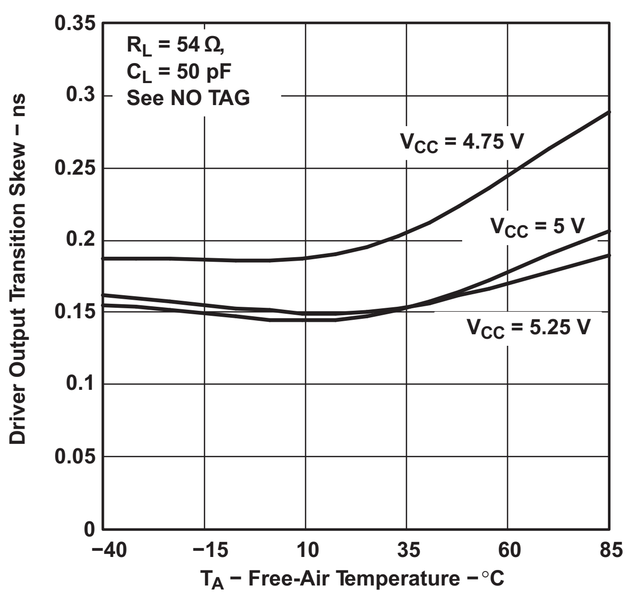


Figure 18.

DRIVER RISE, FALL TIME
vs
FREE-AIR TEMPERATURE

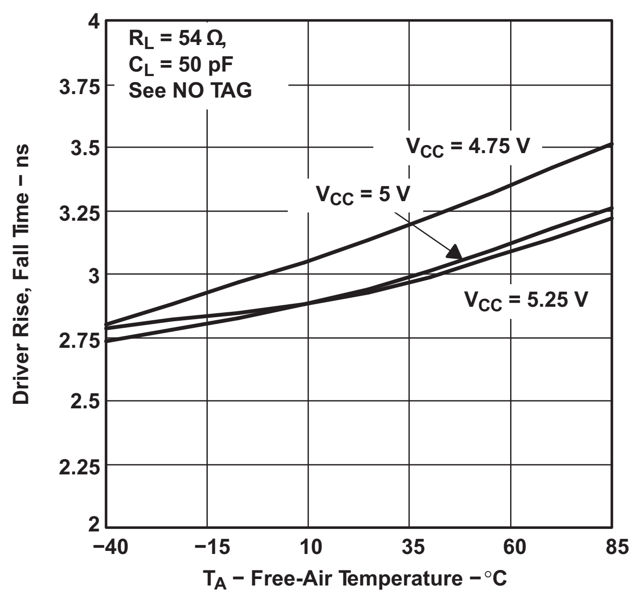


Figure 19.

TYPICAL CHARACTERISTICS (continued)

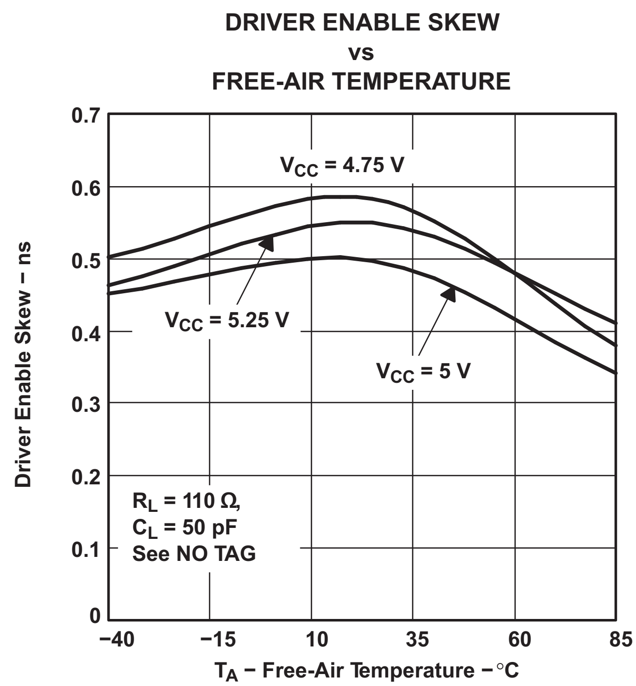


Figure 20.

APPLICATION INFORMATION

Thermal Characteristics of IC Packages

θ_{JA} (**Junction-to-Ambient Thermal Resistance**) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is *not* a constant and is a strong function of:

- PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives *best case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

θ_{JC} (**Junction-to-Case Thermal Resistance**) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is not a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (**Junction-to-Board Thermal Resistance**) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card. θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 21).

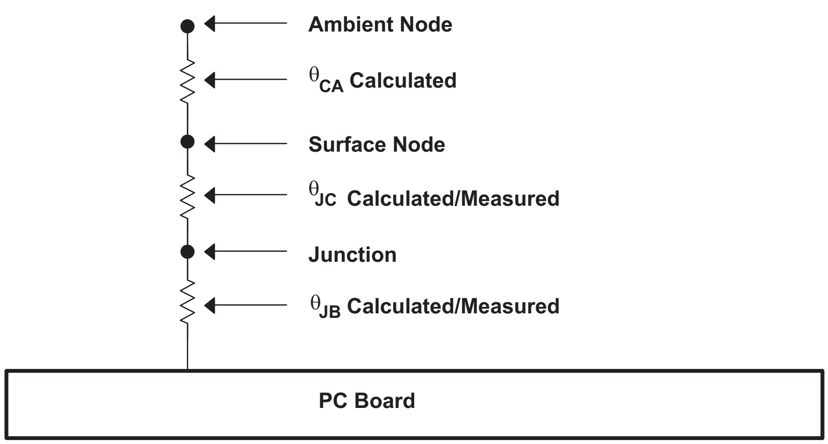


Figure 21. Thermal Resistance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65HVD1176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD1176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD1176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD1176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD1176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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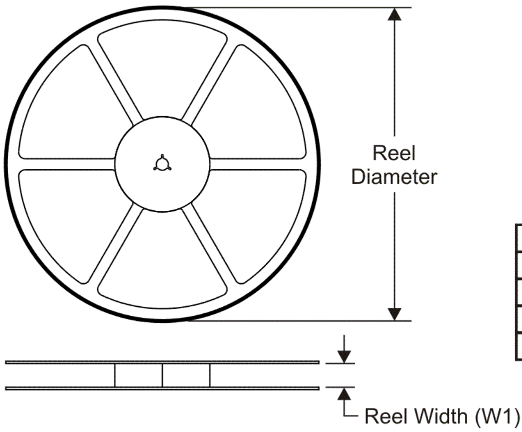
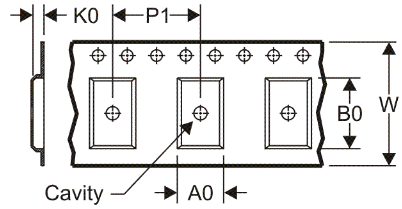
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

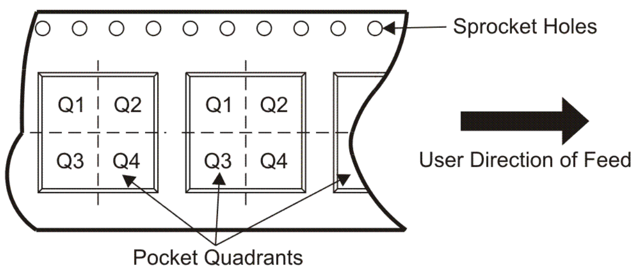


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

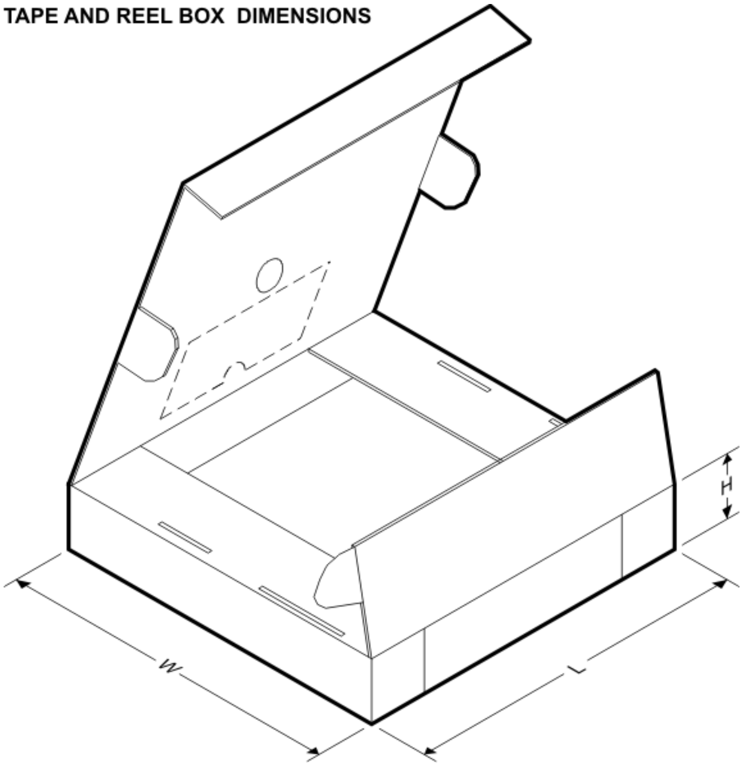
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

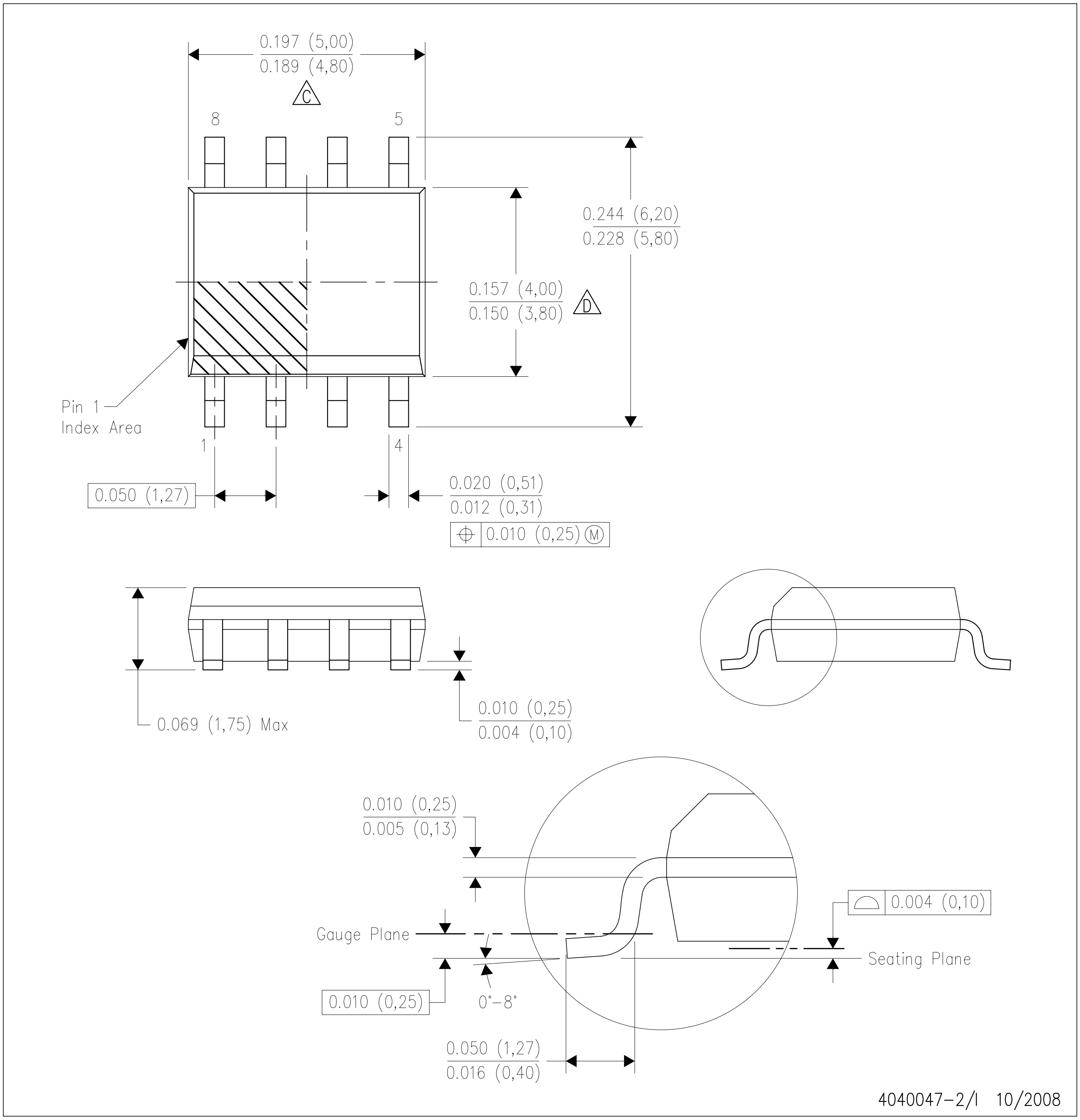
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1176DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75HVD1176DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

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